processor across said channel, said first and second processors selected from one or more of a plurality of processor types.

72. The method of Claim 71, wherein said plurality of processor types consists of Cathedral-III processors, ARM processors and VHDL generated processors.

73. The method recited in Claim 56, wherein said communication channels are implemented in software for communications between a first processor and a second processor across said channel, said first and second processors selected from one or more of a plurality of processor types.

74. The method recited in Claim 56, wherein said communication channels are implemented in a combination of hardware and software, for communications between a first processor and a second processor across said channel, said first and second processors selected from one or more of a plurality of processor types.

75. The method recited in Claim 57, wherein said step of partitioning involves defining a library of auxiliary processes to simulate the digital system, the library of processes selected from a plurality of processes.

76. The method of Claim 75, wherein said plurality of processes consists of one or more of an interactive I/O process, a file I/O process, a graphical output process, a channel duplicator process, a channel merging process, a FF. process, a slider process, a button process, a first-in, first-out buffer process, an ARM processor, a digital to analog conversion process and an analog to digital conversion process.

REMARKS

New Claims 41-76 corresponding substantially to prior Claims 1-20. However, Claims 41 and 54 reflect amendments different from those last proposed in the parent case made to distinctly claim the subject matter but not alter the scope. New Claims 41 and 54 are distinct from the previously cited art. U.S. Patent No. 5,742,840 at Col. 11:19-41 describes a single general purpose media processor, handling the data stream with the same time by the same processor. The '840 patent, at Col. 3:41-43, emphasizes the use of a **unified** processor and teaches against heterogeneous combinations of processors. The method of the claims offers a

generic way to connect different parts — subsystems or processors — defining large and complex systems being heterogeneous in nature (Description, p. 12, Line 4-6).

The '840 patent describes a method for communication between a general purpose media processor and external devices being organized within a communication network and connected via communication fabrics such as fiber optic cable, coaxial cable and twisted pair wires. Col. 6:19. The general purpose media processor is partitionable in some sense.

The '840 patent does not disclose the presently claimed invention. New Claims 41 and 54 describe partitioning of a digital system into a plurality of processes and communication between said processes. If one considers the general purpose media processor in the '840 patent, the partitionable digital system, it is evident that the communication is of a different nature (communication between the general purpose media processor or partitionable digital system and external devices) than in Claims 41 and 54 (communication between the processes wherein said general purpose media processor or partitional digital system is partitioned). If one considers the general purpose media processor of the '840 patent and the external devices as the processes and/or processors, it is evident that partitioning one of such processors is meant, while in Claim 41 and 54, the digital system itself is partitioned. Moreover, the partitionable feature within of the '840 patent is related to handling of various type of media streams, which in not the case in Claims 41 and 54. Moreover, as Claims 41 and 54 relate to a design or implementation method for digital systems, it is clear that communications of a totally different level, e.g., on a single chip or on a PCB board is meant, **within the digital system**, not long distance communication as over a fiber optic, coaxial cable and twisted pair wires.

The Examiner in the parent case relates the memory aspect of the communication channels to effects such as noise and echo, induced by physical phenomena. These memory effects are of a physical long distance channel phenomena, not memory. The memory less or memory free communication channel of Claim 41 and 54 refers to the absence of storage within the short communication channel. The proposed communication approach avoids the need for large buffers or storage capacities within the digital system as this would lead to less area-efficient implementations. The '840 patent cannot be understood as presenting memory-less communication channels and communication approaches avoiding storage requirements to deal with communication mismatches between processors.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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Dated: 1/10/01

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